0.9-V to 6.5-V, Nanopower Comparator

Check for Samples: TLV3691

FEATURES

- **Low Quiescent Current: 75 nA**
- **Wide Supply:**
  - **+0.9 V to +6.5 V**
  - **±0.45 V to ±3.25 V**
- **microPackages: DFN-6 (1 mm × 1 mm), SC70-5**
- **Input Common-Mode Range Extends 100 mV Beyond Both Rails**
- **Response Time: 24 µs**
- **Low Input Offset Voltage: ±3 mV**
- **Push-Pull Output**
- **Industrial Temperature Range: –40°C to +125°C**

APPLICATIONS

- **Over- and Undervoltage Detection**
- **Window Comparators**
- **Overcurrent Detection**
- **Zero-Crossing Detection**
- **System Monitoring:**
  - **Smart Phones**
  - **Tablets**
  - **Industrial Sensors**
  - **Portable Medical**

DESCRIPTION

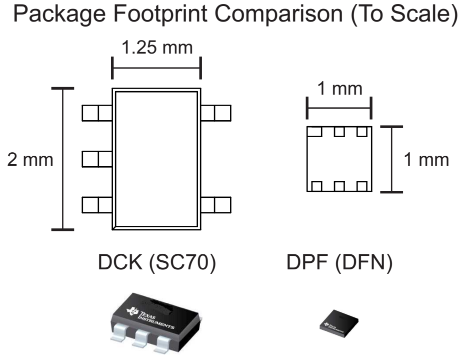
The TLV3691 offers a wide supply range, low quiescent current, and rail-to-rail inputs. All of these features come in industry-standard and extremely small packages, making this device an excellent choice for low-voltage and low-power applications.

Available as a single channel, the low-power, wide supply and temperature range makes this device flexible enough to handle almost any application from consumer to industrial. The TLV3691 is available in SC70-5 and 1-mm × 1-mm DFN-6 packages. This device is specified for operation across the expanded industrial temperature range of –40°C to +125°C.

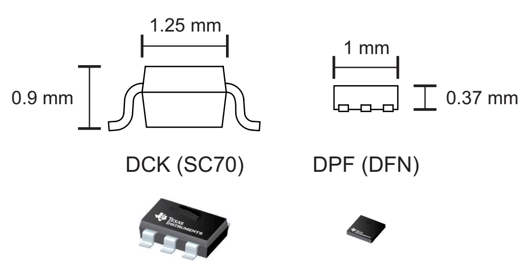
RELATED PRODUCTS

FEATURES	DEVICE
40-ns, 40-µA, push-pull comparator	TLV3201
	TLV3202
4.5-ns, rail-to-rail, high-speed comparator	TLV3501
	TLV3502
Nanopower push-pull output comparator	TLV3491
	TLV3492
	TLV3494
3.9-µA, SC70-3 voltage reference	REF3312
	REF3318
	REF3320
	REF3325
	REF3330
	REF3333

Package Footprint Comparison (To Scale)



Package Height Comparison (To Scale)



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

		MIN	MAX	UNIT
Supply voltage			+7	V
Signal input terminals	Voltage(2)	(V–) – 0.5	(V+) + 0.5	V
	Current(2)		±10	mA
Output short-circuit(3)		continuous		mA
Temperature	Operating, T_A	–55	+150	°C
	Storage, T_{stg}	–65	+150	°C
	Junction, T_J		+150	°C
Electrostatic discharge (ESD) ratings	Human body model (HBM)		2.5	kV
	Charged-device model (CDM)		1	kV

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current-limited to 10 mA or less.
(3) Short-circuit to ground, one comparator per package.

THERMAL INFORMATION

THERMAL METRIC(1)		TLV3691		UNITS
		DCK (SC70)	DPF (DFN)	
		5 PINS	6 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	297.4	252.4	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	109.3	93.9	
θ_{JB}	Junction-to-board thermal resistance	74.4	192.8	
ψ_{JT}	Junction-to-top characterization parameter	3.0	3.0	
ψ_{JB}	Junction-to-board characterization parameter	73.6	203.8	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ELECTRICAL CHARACTERISTICS: V_S = +0.9 V to +6.5 V

At T_A = +25°C, V_S = +0.9 V to +6.5 V, V_{CM} = V_S/2 and C_L = 15 pF, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage			±3	±15	mV
		T_A = –40°C to +125°C			±22	mV
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +125°C			±70	µV/°C
PSRR	Power-supply rejection ratio	T_A = –40°C to +125°C			2000	µV/V
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range	T_A = –40°C to +125°C	(V–) – 0.1		(V+) + 0.1	V
	Hysteresis			±17		mV
INPUT BIAS CURRENT						
I_B	Input bias current			30	100	pA
		T_A = –40°C to +125°C			20	nA
I_{OS}	Input offset current			8		pA
C_{LOAD}	Capacitive load drive		See Typical Characteristics			
OUTPUT						
V_{OH}	Voltage output swing from upper rail	I_O = 2.5 mA, input overdrive ≥ 50 mV, V_S = 6.5 V		155	165	mV
		I_O = 2.5 mA, input overdrive ≥ 50 mV, V_S = 6.5 V, T_A = –40°C to +125°C			220	mV
		I_O ≤ 100 µA, input overdrive ≥ 50 mV, V_S = 6.5 V		6	10	mV
		I_O ≤ 100 µA, input overdrive ≥ 50 mV, V_S = 6.5 V, T_A = –40°C to +125°C			20	mV
		I_O ≤ 100 µA, input overdrive ≥ 50 mV, V_S = 0.9 V		70	75	mV
		I_O ≤ 100 µA, input overdrive ≥ 50 mV, V_S = 0.9 V, T_A = –40°C to +125°C			80	mV
V_{OL}	Voltage output swing from lower rail	I_O = 2.5 mA, input overdrive ≥ 50 mV, V_S = 6.5 V		155	165	mV
		I_O = 2.5 mA, input overdrive ≥ 50 mV, V_S = 6.5 V, T_A = –40°C to +125°C			220	mV
		I_O ≤ 100 µA, input overdrive ≥ 50 mV, V_S = 6.5 V		6	10	mV
		I_O ≤ 100 µA, input overdrive ≥ 50 mV, V_S = 6.5 V, T_A = –40°C to +125°C			20	mV
		I_O ≤ 100 µA, input overdrive ≥ 50 mV, V_S = 0.9 V		35	40	mV
		I_O ≤ 100 µA, input overdrive ≥ 50 mV, V_S = 0.9 V, T_A = –40°C to +125°C			45	mV
I_{SC}	Short circuit sink current	V_S = 6.5 V, see Typical Characteristics		42		mA
	Short circuit source current	V_S = 6.5 V, see Typical Characteristics		35		mA

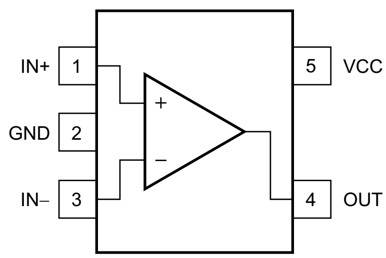
ELECTRICAL CHARACTERISTICS: V_S = +0.9 V to +6.5 V (continued)

At T_A = +25°C, V_S = +0.9 V to +6.5 V, V_{CM} = V_S/2 and C_L = 15 pF, unless otherwise noted.

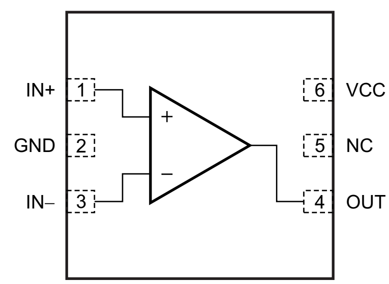
PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SWITCHING CHARACTERISTICS							
t_{PHL}	Propagation delay time	High to low	V_S = 6.5 V, Input overdrive = 50 mV		32		µs
			V_S = 0.9 V, Input overdrive = 50 mV		45		µs
			V_S = 6.5 V, Input overdrive = 100 mV		24		µs
			V_S = 0.9 V, Input overdrive = 100 mV		35		µs
t_{PLH}		Low to high	V_S = 6.5 V, Input overdrive = 50 mV		32		µs
			V_S = 0.9 V, Input overdrive = 50 mV		40		µs
			V_S = 6.5 V, Input overdrive = 100 mV		24		µs
			V_S = 0.9 V, Input overdrive = 100 mV		28		µs
t_R	Rise time		Input overdrive = 100 mV		330		ns
t_F	Fall time		Input overdrive = 100 mV		330		ns
POWER SUPPLY							
V_S	Specified voltage range			0.9		6.5	V
I_Q	Quiescent current (per channel)				75	150	nA
			T_A = –40°C to +125°C			200	nA
TEMPERATURE RANGE							
	Specified range			–40		+125	°C
	Operating range			–55		+150	°C
	Storage range			–65		+150	°C

PIN CONFIGURATIONS

DCK PACKAGE
SC70-5
(TOP VIEW)



DPF PACKAGE
DFN-6
(TOP VIEW)



NOTE: NC = no connection.

TYPICAL CHARACTERISTICS

At T_A = +25°C, V_S = +0.9 V to +6.5 V, and input overdrive = 100 mV, unless otherwise noted.

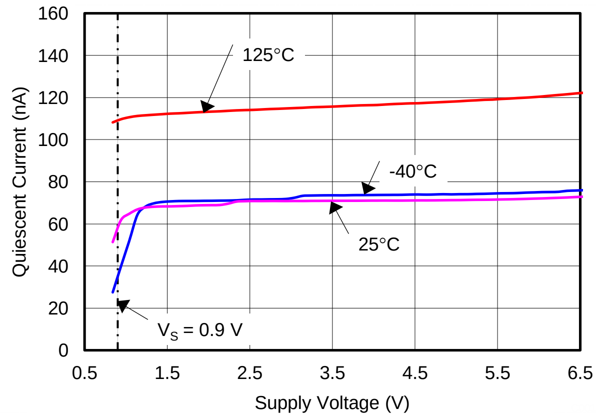


Figure 1. QUIESCENT CURRENT vs SUPPLY VOLTAGE

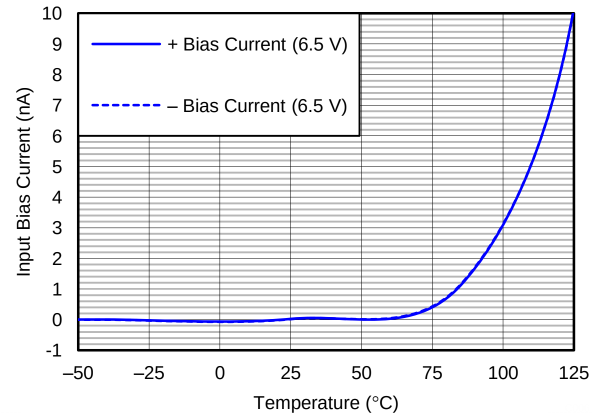


Figure 2. INPUT BIAS CURRENT vs TEMPERATURE

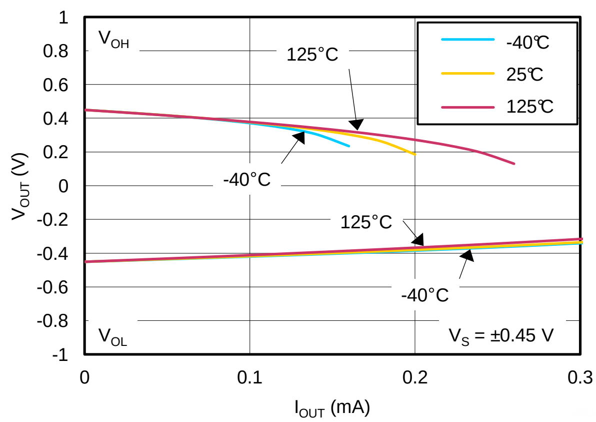


Figure 3. OUTPUT VOLTAGE vs OUTPUT CURRENT (V_S = 0.9 V)

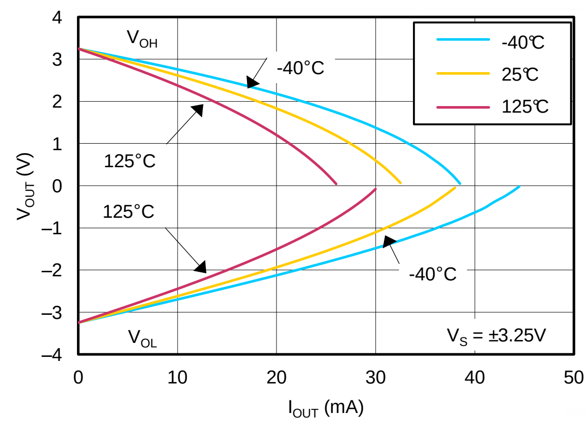


Figure 4. OUTPUT VOLTAGE vs OUTPUT CURRENT (V_S = 6.5 V)

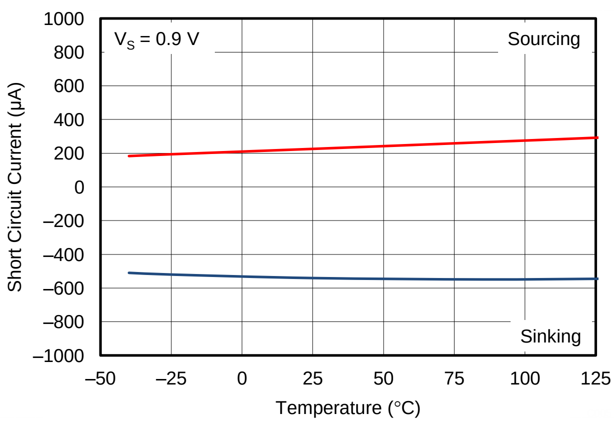


Figure 5. SHORT-CIRCUIT CURRENT vs TEMPERATURE (V_S = 0.9 V)

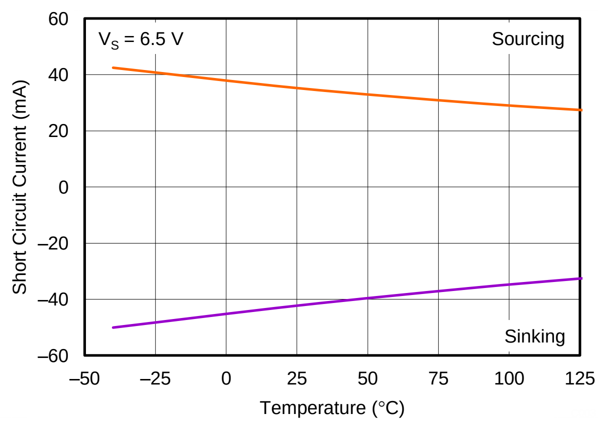


Figure 6. SHORT-CIRCUIT CURRENT vs TEMPERATURE (V_S = 6.5 V)

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = +0.9 V to +6.5 V, and input overdrive = 100 mV, unless otherwise noted.

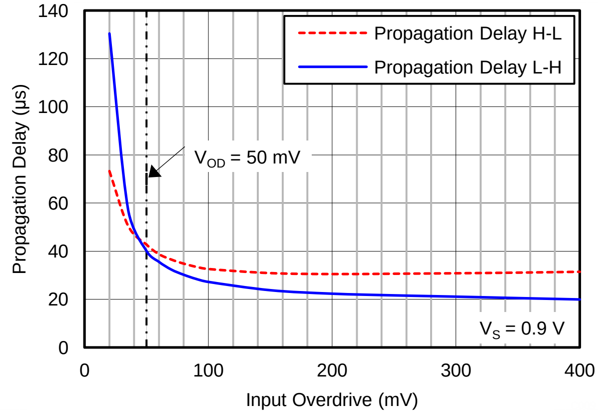


Figure 7. PROPAGATION DELAY vs INPUT OVERDRIVE (V_S = 0.9 V)

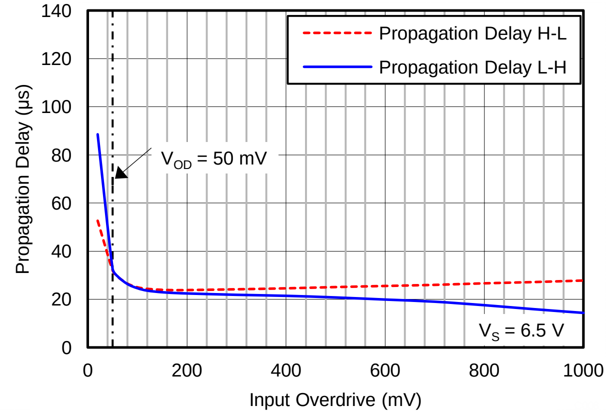


Figure 8. PROPAGATION DELAY vs INPUT OVERDRIVE (V_S = 6.5 V)

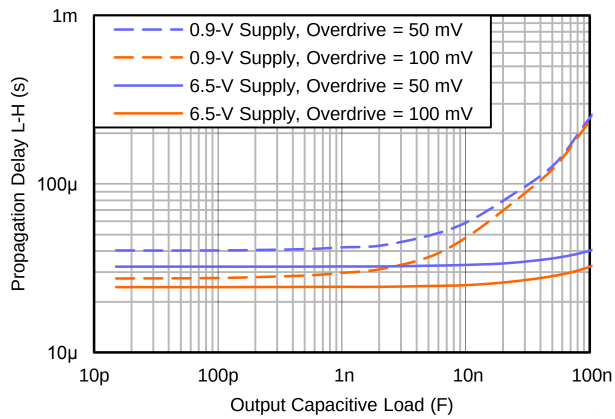


Figure 9. PROPAGATION DELAY (t_{PLH}) vs CAPACITIVE LOAD

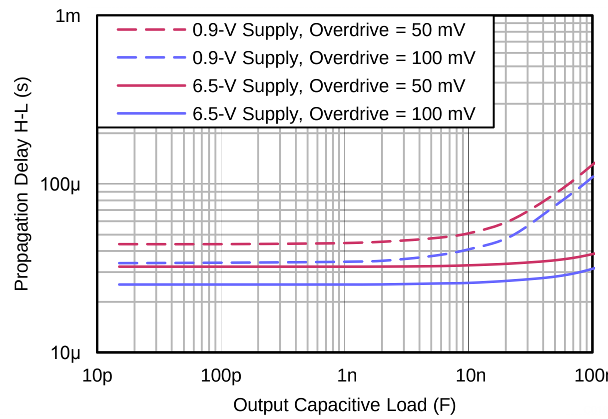


Figure 10. PROPAGATION DELAY (t_{PHL}) vs CAPACITIVE LOAD

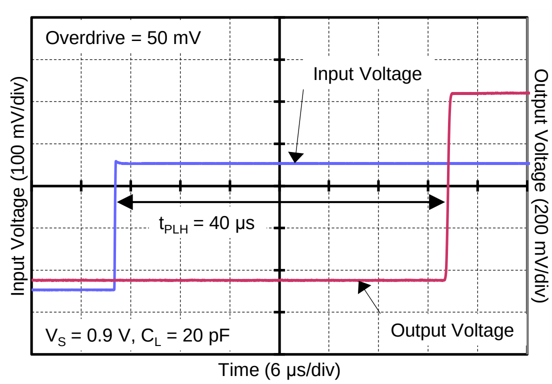


Figure 11. PROPAGATION DELAY (t_{PLH}) (V_S = 0.9 V, Overdrive = 50 mV)

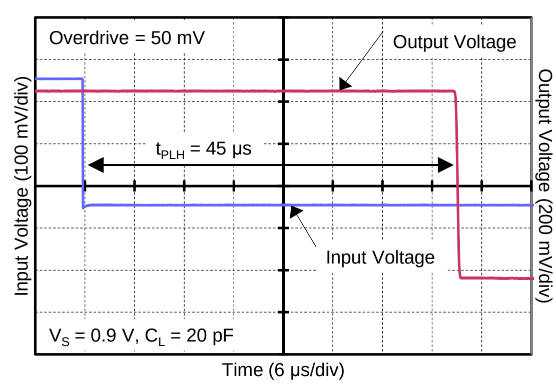


Figure 12. PROPAGATION DELAY (t_{PHL}) (V_S = 0.9 V, Overdrive = 50 mV)

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = +0.9 V to +6.5 V, and input overdrive = 100 mV, unless otherwise noted.

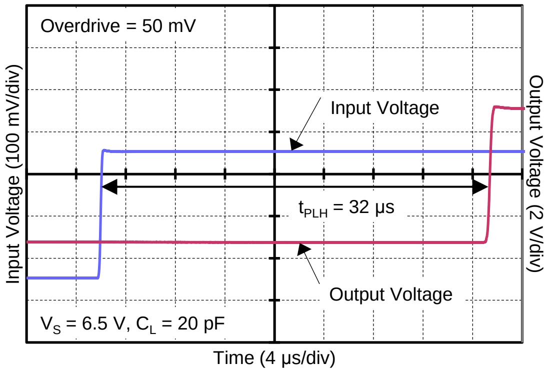


Figure 13. PROPAGATION DELAY (t_{PLH}) (V_S = 6.5 V, Overdrive = 50 mV)

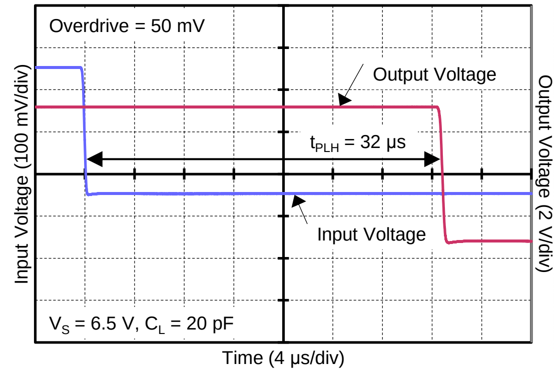


Figure 14. PROPAGATION DELAY (t_{PHL}) (V_S = 6.5 V, Overdrive = 50 mV)

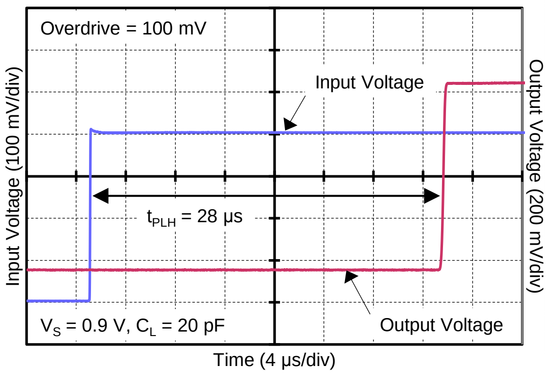


Figure 15. PROPAGATION DELAY (t_{PLH}) (V_S = 0.9 V, Overdrive = 100 mV)

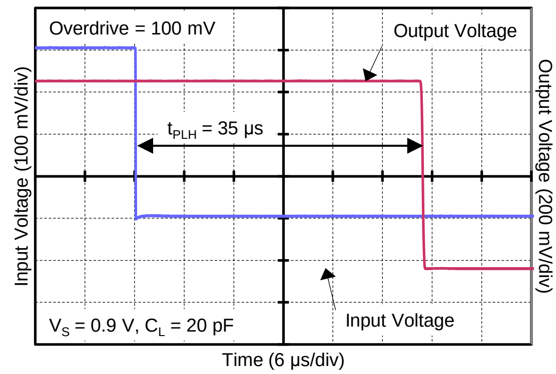


Figure 16. PROPAGATION DELAY (t_{PHL}) (V_S = 0.9 V, Overdrive = 100 mV)

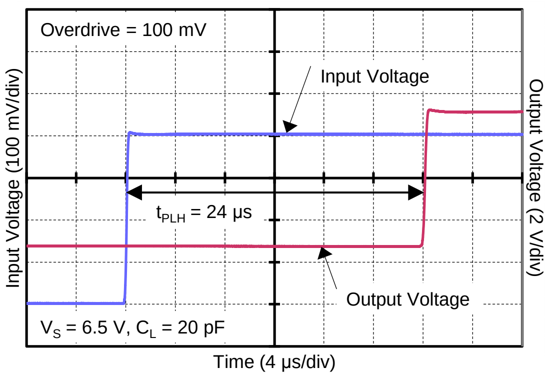


Figure 17. PROPAGATION DELAY (t_{PLH}) (V_S = 6.5 V, Overdrive = 100 mV)

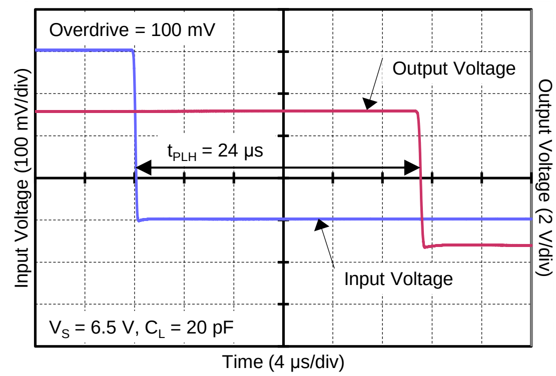


Figure 18. PROPAGATION DELAY (t_{PHL}) (V_S = 6.5 V, Overdrive = 100 mV)

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = +0.9 V to +6.5 V, and input overdrive = 100 mV, unless otherwise noted.

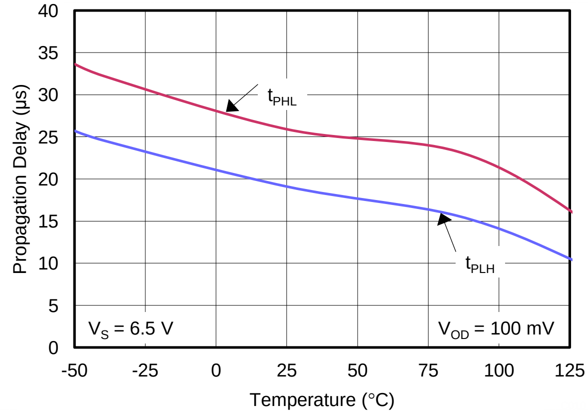


Figure 19. PROPAGATION DELAY vs TEMPERATURE

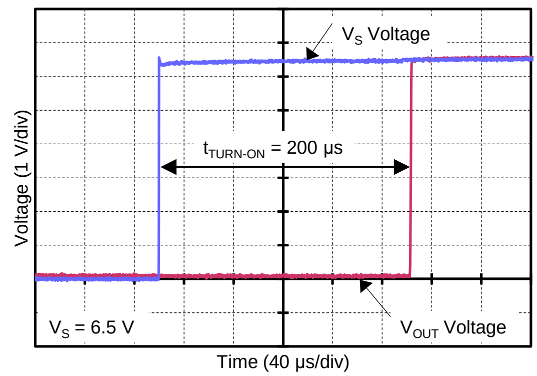


Figure 20. START-UP TIME

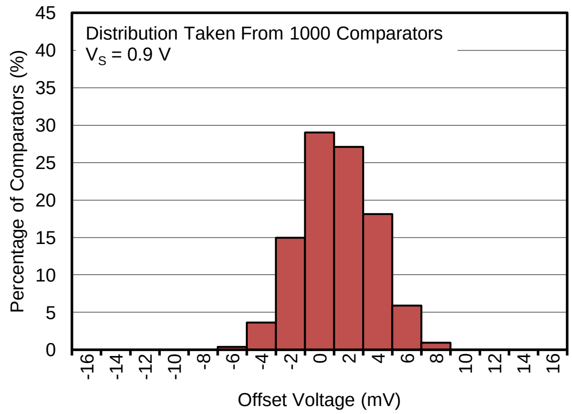


Figure 21. OFFSET VOLTAGE PRODUCTION DISTRIBUTION (V_S = 0.9 V)

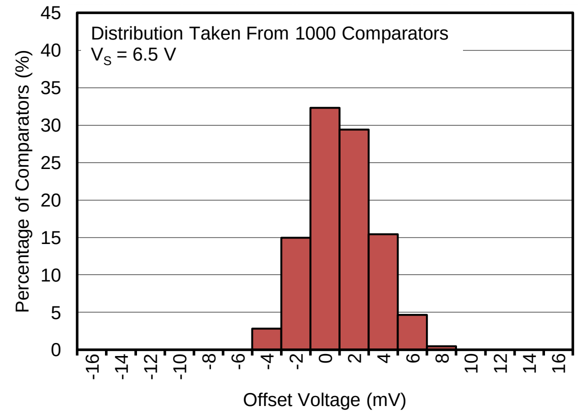


Figure 22. OFFSET VOLTAGE PRODUCTION DISTRIBUTION (V_S = 6.5 V)

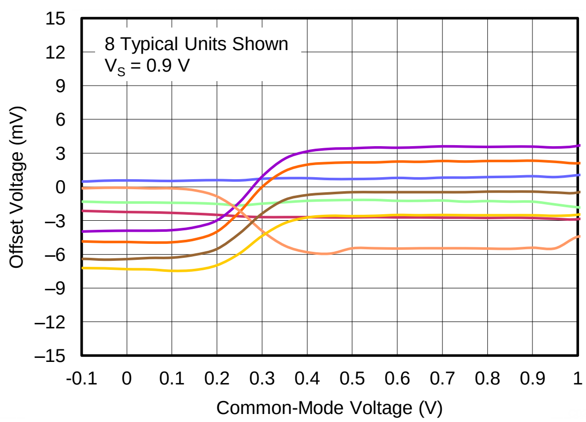


Figure 23. OFFSET VOLTAGE vs COMMON-MODE VOLTAGE (V_S = 0.9 V)

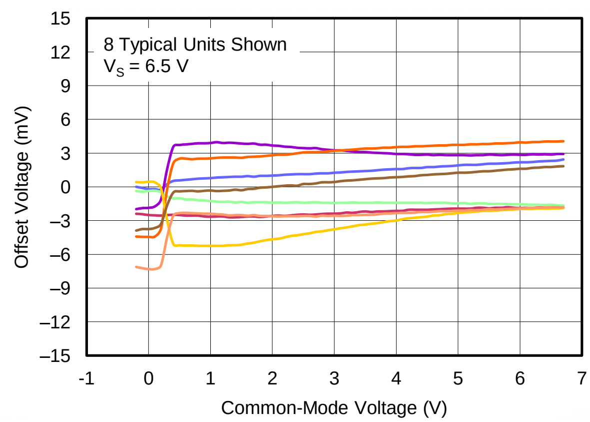


Figure 24. OFFSET VOLTAGE vs COMMON-MODE VOLTAGE (V_S = 6.5 V)

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = +0.9 V to +6.5 V, and input overdrive = 100 mV, unless otherwise noted.

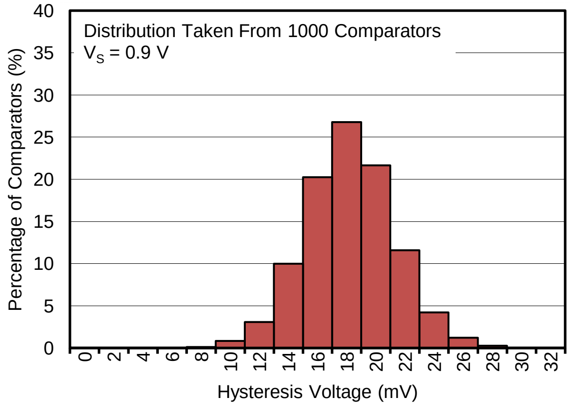


Figure 25. HYSTERESIS PRODUCTION DISTRIBUTION (V_S = 0.9 V)

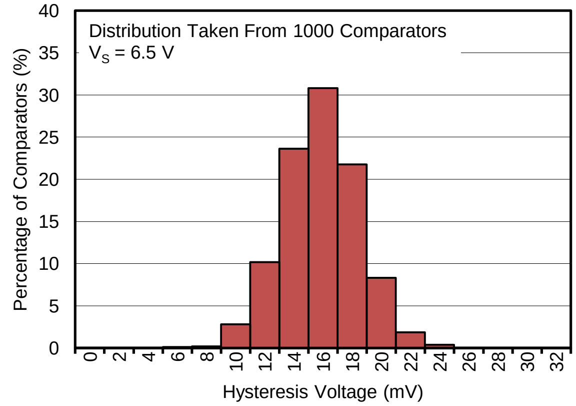


Figure 26. HYSTERESIS PRODUCTION DISTRIBUTION (V_S = 6.5 V)

APPLICATION INFORMATION

The TLV3691 comparators feature rail-to-rail inputs and outputs on supply voltages as low as 0.9 V. The push-pull output stage is optimal for reduced power budget applications and features no shoot-through current. Low minimum supply voltages, common-mode input range beyond supply rails, and a typical supply current of 75 nA make the TLV3691 an excellent candidate for battery-operated and portable, handheld designs.

COMPARATOR INPUTS

The TLV3691 is a rail-to-rail input comparator, with an input common-mode range that exceeds the supply rails by 100 mV for both positive and negative supplies. The device is designed to prevent phase inversion when the input pins exceed the supply voltage. Figure 27 shows the device response when input voltages exceed the supply, resulting in no phase inversion.

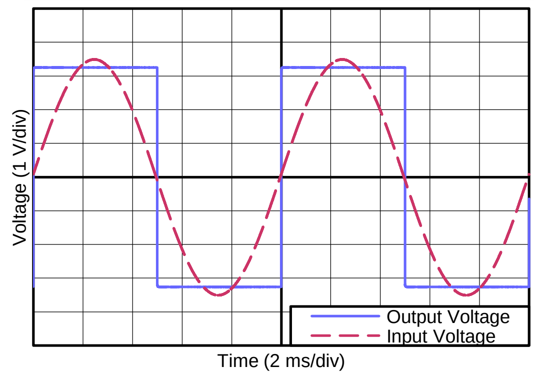


Figure 27. No Phase Inversion: Comparator Response to Input Voltage (Propagation Delay Included)

EXTERNAL HYSTERESIS

The device hysteresis transfer curve is shown in Figure 28. This curve is a function of three components: V_{TH}, V_{OS}, and V_{HYST}.

- V_{TH} is the actual set voltage or threshold trip voltage.
- V_{OS} is the internal offset voltage between V_{IN+} and $V_{IN–}$. This voltage is added to V_{TH} to form the actual trip point at which the comparator must respond in order to change output states.
- V_{HYST} is the internal hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise (17 mV for the TLV3691).

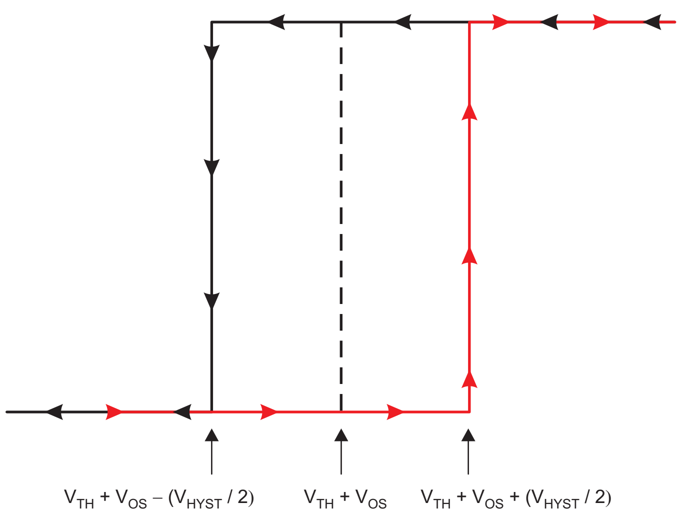


Figure 28. Hysteresis Transfer Curve

Inverting Comparator With Hysteresis

The inverting comparator with hysteresis requires a three-resistor network that is referenced to the comparator supply voltage (V_{CC}), as shown in Figure 29. When V_{IN} at the inverting input is less than V_A, the output voltage is high (for simplicity, assume V_O switches as high as V_{CC}). The three network resistors can be represented as R1 || R3 in series with R2. The high to low trip voltage (V_{A1}) is defined by Equation 1:

$$V_{A1} = V_{CC} \times \frac{R2}{(R1 \,||\, R3) + R2} \quad (1)$$

When V_{IN} is greater than V_A, the output voltage is low, very close to ground. In this case, the three network resistors can be presented as R2 || R3 in series with R1. The low to high trip voltage (V_{A2}) is defined by Equation 2:

$$V_{A2} = V_{CC} \times \frac{R2 \,||\, R3}{R1 + (R2 \,||\, R3)} \quad (2)$$

The total hysteresis provided by the network is defined by Equation 3:

$$\Delta V_A = V_{A1} - V_{A2} \quad (3)$$

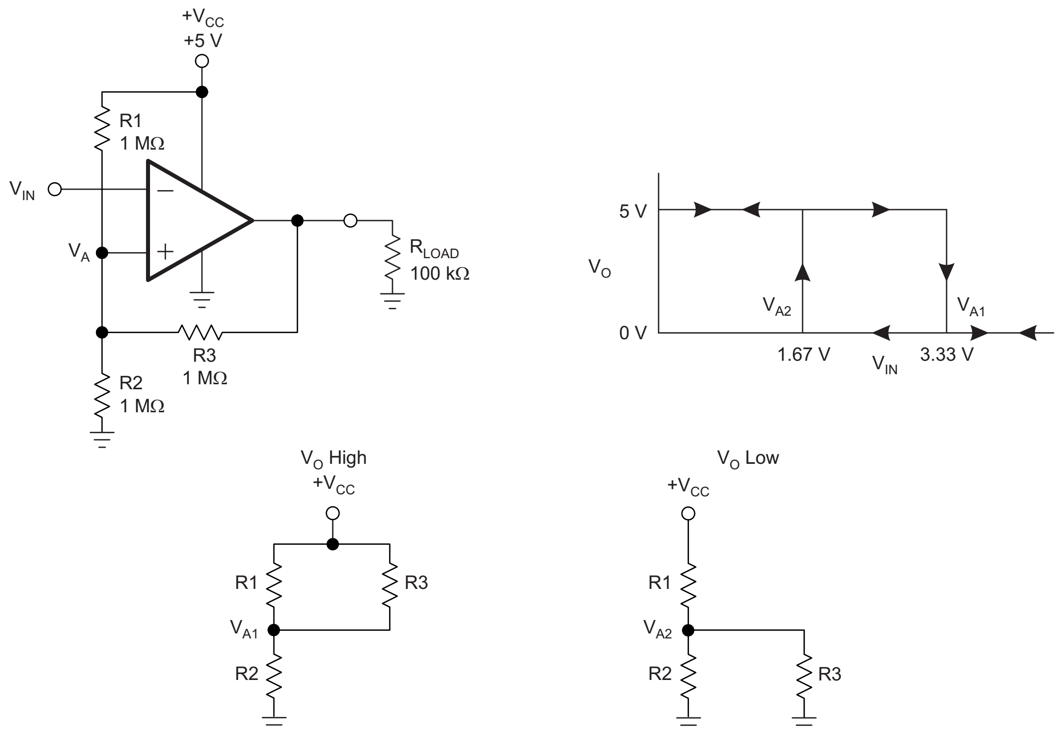


Figure 29. TLV3691 in an Inverting Configuration with Hysteresis

Noninverting Comparator with Hysteresis

A noninverting comparator with hysteresis requires a two-resistor network, as shown in Figure 30, and a voltage reference (V_{REF}) at the inverting input. When V_{IN} is low, the output is also low. For the output to switch from low to high, V_{IN} must rise to V_{IN1}. V_{IN1} is calculated by Equation 4:

$$V_{IN1} = R1 \times \frac{V_{REF}}{R2} + V_{REF} \quad (4)$$

When V_{IN} is high, the output is also high. In order for the comparator to switch back to a low state, V_{IN} must drop to V_{IN2} such that V_A is equal to V_{REF}. V_{IN2} can be calculated by Equation 5:

$$V_{IN2} = \frac{V_{REF}(R1 + R2) - V_{CC} \times R1}{R2} \quad (5)$$

The hysteresis of this circuit is the difference between V_{IN1} and V_{IN2}, as defined by Equation 6.

$$\Delta V_{IN} = V_{CC} \times \frac{R1}{R2} \quad (6)$$

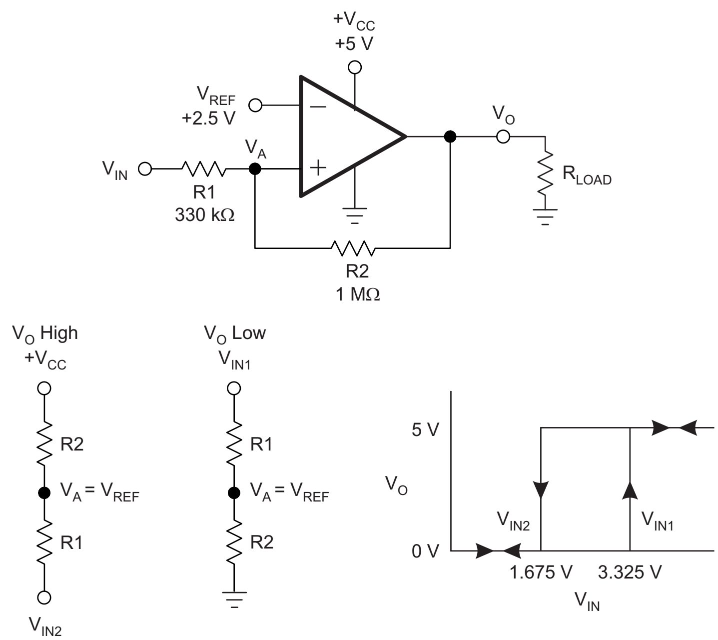


Figure 30. TLV3691 in a Noninverting Configuration with Hysteresis

CAPACITIVE LOADS

Under reasonable capacitive loads, the device maintains specified propagation delay (see the Typical Characteristics). However, excessive capacitive loading under high switching frequencies may increase supply current, propagation delay, or induce decreased slew rate.

CIRCUIT LAYOUT

Comparators are very sensitive to input noise. For best results, the following layout guidelines should be maintained:

1. Use a printed circuit board (PCB) with a good, unbroken, low-inductance ground plane. Proper grounding (use of a ground plane) helps maintain specified device performance.
2. To minimize supply noise, place a decoupling capacitor (0.1-μF ceramic, surface-mount capacitor) as close as possible to V_{CC}.
3. On the inputs and the output, keep lead lengths as short as possible to avoid unwanted parasitic feedback around the comparator. Keep inputs away from the output.
4. Solder the device directly to the PCB rather than using a socket.
5. For slow-moving input signals, take care to prevent parasitic feedback. A small capacitor (1000 pF or less) placed between the inputs can help eliminate oscillations in the transition region. This capacitor causes some degradation to propagation delay when impedance is low. The topside ground plane runs between the output and inputs.
6. The ground pin ground trace runs under the device up to the bypass capacitor, shielding the inputs from the outputs.

SETTING THE REFERENCE VOLTAGE

Using a stable reference when setting the transition point for the device is important. The REF3312, as shown in Figure 31, provides a 1.25-V reference voltage with low drift and only 3.9 μA of quiescent current.

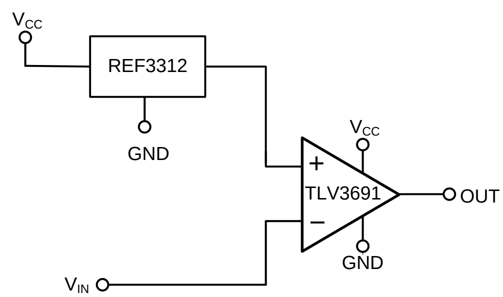


Figure 31. Reference Voltage for the TLV3691

APPLICATIONS

This section provides several example applications for the TLV3691.

Over- and Undervoltage Detection

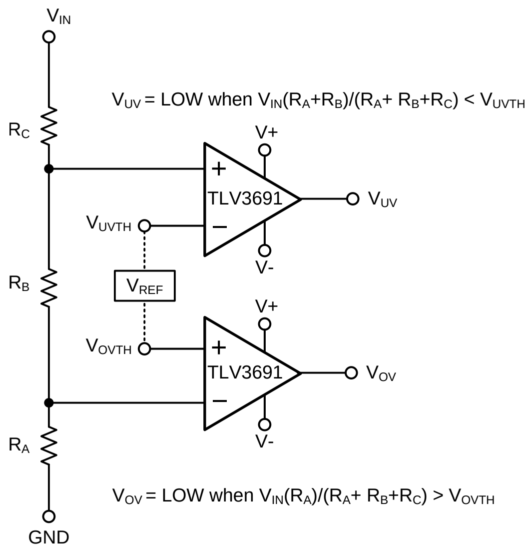


Figure 32. Over- and Undervoltage Detection

System Monitoring

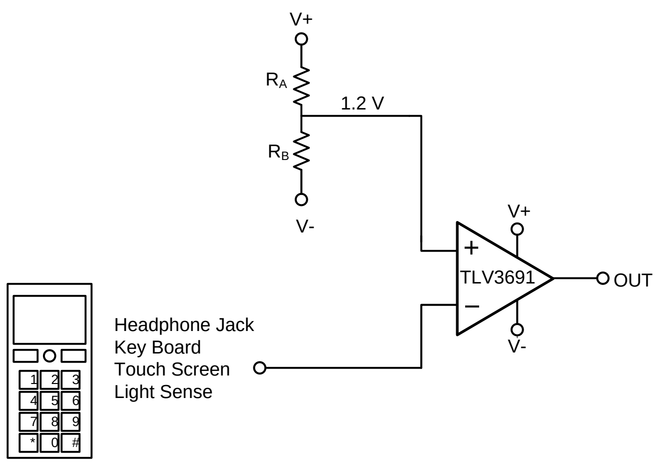


Figure 33. System Monitoring

Window Comparator

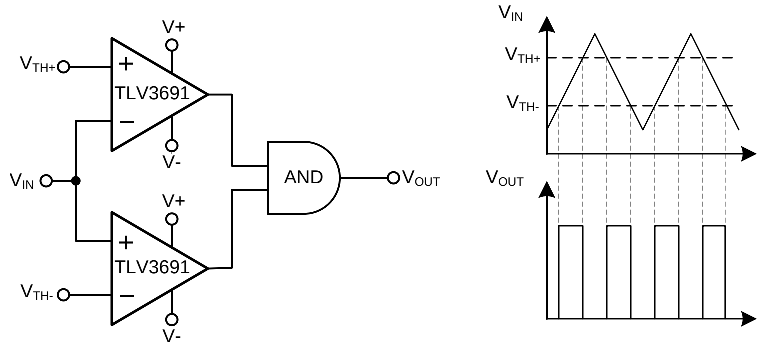


Figure 34. Window Comparator

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV3691IDCKR	ACTIVE	SC70	DCK	5	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SIV	Samples
TLV3691IDCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SIV	Samples
TLV3691IDPFR	ACTIVE	X2SON	DPF	6	5000	TBD	Call TI	Call TI	-40 to 125		Samples
TLV3691IDPFT	ACTIVE	X2SON	DPF	6	250	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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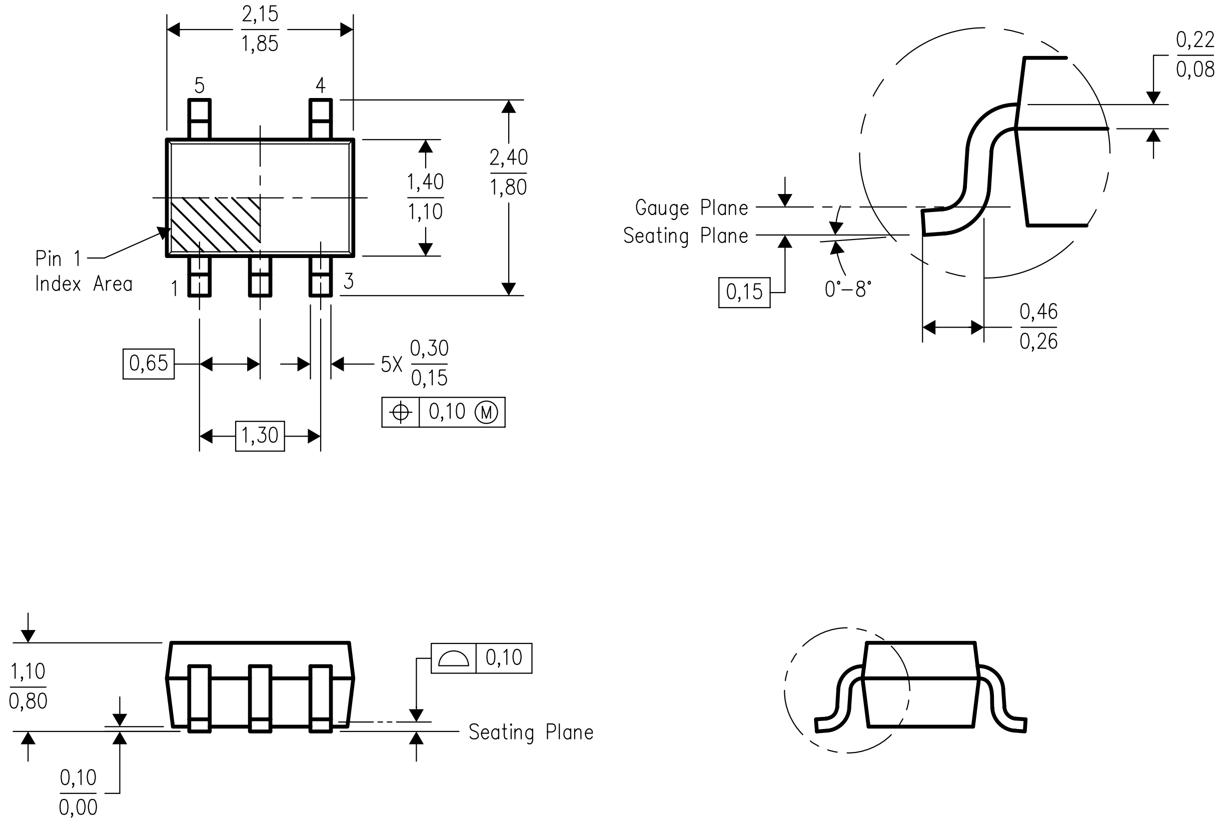

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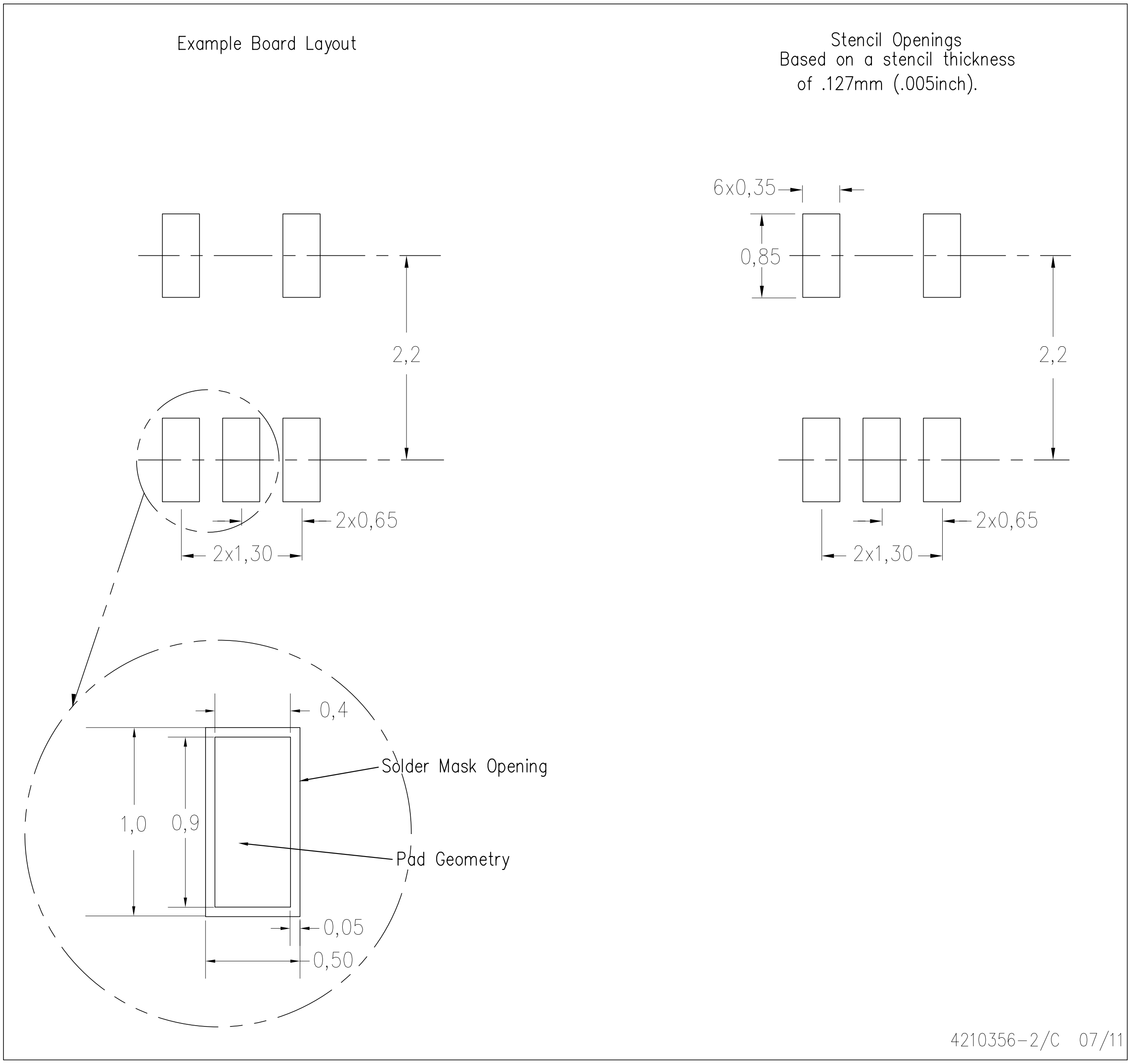
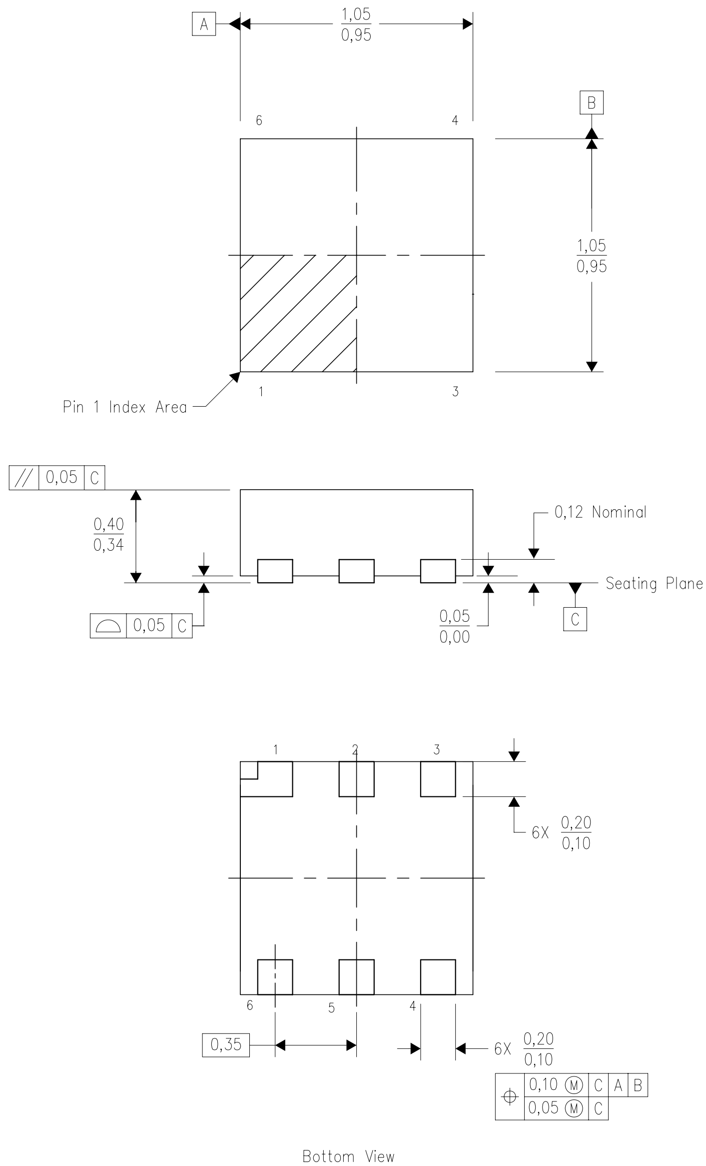
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-203 variation AA.

DCK (R-PDSO-G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DPF (S-PX2SON-N6) PLASTIC SMALL OUTLINE NO-LEAD



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NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. SON (Small Outline No-Lead) package configuration.

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